Digital Logic Design (CS302)
Final Term Exam

Total marks = 80

Date
17th of Feb 2018

Objectives 40 Marks

1. The address from which the data is read, is provided by _____

- Depends on circuitry
- None of given options
- RAM
- **Microprocessor**

2. The best state assignment tends to _____.

- Maximizes the number of state variables that don't change in a group of related states
- **Minimizes the number of state variables that don't change in a group of related states**
- Minimize the equivalent states
- None of given options

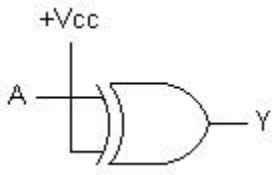
3. The total amount of memory that is supported by any digital system depends upon _____

- The organization of memory
- The structure of memory
- The size of decoding unit
- **The size of the address bus of the microprocessor**

4. The expression F=A+B+C describes the operation of three bits _____ Gate.

- **OR**
- AND
- NOT
- NAND

5. The output of this circuit is always _____.



- 1
- 0
- **A**
- $\overline{A}$

6. A Nibble consists of _____ bits

- 2
- **4**

- 8
- 16

7. In asynchronous transmission when the transmission line is idle, _____

- It is set to logic low
- It is set to logic high
- Remains in previous state
- State of transmission line is not used to start transmission

8. The _____ input overrides the _____ input

- Asynchronous, synchronous
- Synchronous, asynchronous
- Preset input (PRE), Clear input (CLR)
- Clear input (CLR), Preset input (PRE)

9. In a sequential circuit the next state is determined by _____ and _____

- State variable, current state
- Current state, flip-flop output
- **Current state and external input**
- Input and clock signal applied

10. A 8-bit serial in / parallel out shift register contains the value "8", _____ clock signal(s) will be required to shift the value completely out of the register.

- 1
- 2
- 4
- **8**

11. The 4-bit 2's complement representation of "+5" is _____

- 1010
- 1110
- 1011
- **0101**

12. Stack is an acronym for _____

- FIFO memory
- **LIFO memory**
- Flash Memory
- Bust Flash Memory

13. FIFO is an acronym for _____

- **First In, First Out**
- Fly in, Fly Out
- Fast in, Fast Out
- None of given options

14. DRAM stands for _____

- **Dynamic RAM**
- Data RAM
- Demoduler RAM
- None of given options

15. The alternate solution for a DE multiplexer-register combination circuit is _____

- Parallel in / Serial out shift register
- Serial in / Parallel out shift register
- Parallel in / Parallel out shift register
- Serial in / Serial Out shift register

16. In a state diagram, the transition from a current state to the next state is determined by

- **Current state and the inputs**
- Current state and outputs
- Previous state and inputs
- Previous state and outputs

17. _____ Counters as the name indicates are not triggered simultaneously.

- Asynchronous
- Synchronous
- Positive-Edge triggered
- Negative-Edge triggered

18. "A + B = B + A" is _____

- DE Morgan's Law
- Distributive Law
- **Commutative Law**
- Associative Law

19. For a positive edge-triggered J-K flip-flop with both J and K HIGH, the outputs will _____ if the clock goes HIGH.

- Toggle
- Set
- Reset
- Not change

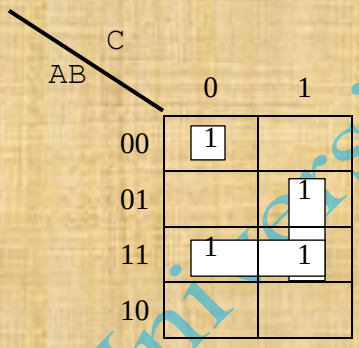
Subjective

5 Questions Each have 3 Marks.

Q # 41:
Two state assignments are given in the table below. Identify which state assignment is best and why?

States	State assignment 1	State assignment 2
A	00	00
B	01	01
C	11	10
D	10	11

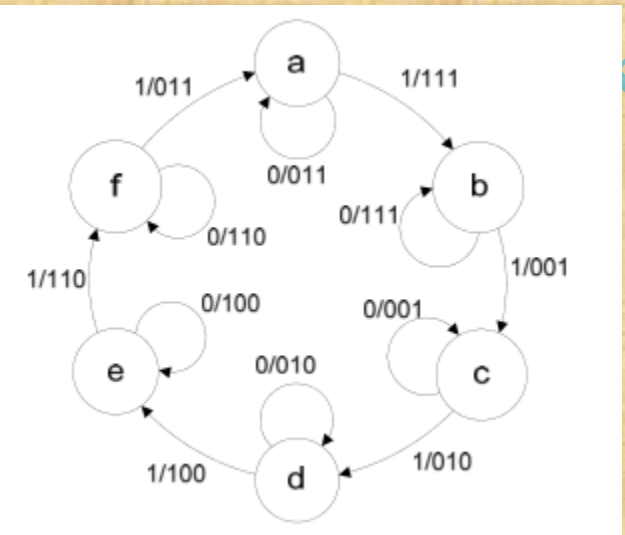
Q # 42:
Determine the SOP Expression for Karnaugh map given below



Q # 43:
Draw the Symbol of Operational Amplifier (Op-Amp).
Q # 44:
Write the Difference b/w Counter and Shift register?
Q # 55:
What are the modes in which a D-Latch Operations?

5 Questions Each have 5 marks:

Q # 46:
Give Function Table of 8 Input Multiplexer using two 4 Input Multiplexer.
Q # 47:
Two Input Combination for which the gated S-R Latch maintain its previous state?
Q # 48:
This is State diagram of a Mealy Machine. Draw the Next State Table of Mealy Machine and showing Present State, Next State, Input and Output.



Q # 49:
Write The Test Vector Definition of 3-bit Up/Down Counter.
Q # 50:
Write the answer as Yes or No in Column C.

Column A	Column B	Column C
SRAM	One-Transistor Cell	
EEPROM	High Density	
ROM	In-System Write ability	
DRAM	Non-Volatile	